IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 8, August 2016

Design of QPSK Digital Modulation Scheme Using Turbo Codes for an Air Borne System

D. Sai Brunda[1], B. Geetha Rani[2]

Student, Department of ECE, G. Pullaiah College of Engineering and Technology, Kurnool, India [1]

Assistant Professor, Department of ECE,G. Pullaiah College of Engineering and Technology, Kurnool, India [2]

Abstract: The demand for wireless communication is more prevalent with its increasing sophistication. The design of QPSK digital modulation scheme emphasizes on turbo encoder, data scrambler, interleaver and modulator which is used to deploy airborne communication between aircraft and ground station as per Consultative Committee for Space Data Systems (CCSDS) standard. The system consists of a digital QPSK modulator circuit. Turbo coder as a powerful coding scheme is used in wireless communication system for encoding the data at the transmission end between the physical layer and data link layer. Turbo decoder is used to decode the data frames at the receiving end. This project has turbo encoding with the bit rate of 1/2 and information block length is 1784 bits, designed using VHDL, simulated using Xilinx ISE simulator and implemented on Xilinx Spartan family FPGA.

Keywords: QPSK Modulation, Turbo Encoder, Data Scrambler, Interleaver.

I. INTRODUCTION

Wireless communication is prevalent everywhere in our day to day life like satellite television, global positioning system (GPS), navigation system, cellular telephones and so many other applications. The digital form of wireless communication is preferred over analog form because of the advantages of digital methods over analog methods. The digital methods are robust, secured, multiplex different forms of data, support error detection and error correction and provide improved performance in the communication system.

The information or signal carrying the data in digital communication is discrete in amplitude and time. At the transmission end, the signals carrying digital data are first converted into analog form before transmitting. This process in known as Modulation. In other words, modulation is defined as the processes of sending a message signal using a high frequency carrier signal for long distance communication. Similarly, the analog signals are converted into digital form at the receiving end which is known as demodulation process.

A.MODULATION TECHNIQUES

The classification of modulation techniques when the message signals are analog and digital are shown in the Fig.1 and Fig.2. The analog signals are modulated using the techniques like amplitude modulation, angle modulation, phase modulation, pulse position modulation, pulse width modulation, pulse amplitude modulation, and pulse code modulation. The digital data are modulated using techniques like amplitude shift keying (ASK), frequency shift keying (FSK), phase shift keying (PSK) where the message signal modulated with respect to amplitude, frequency and phase of carrier signal respectively. The modulation techniques for multi-level discrete data are shown in Fig.3

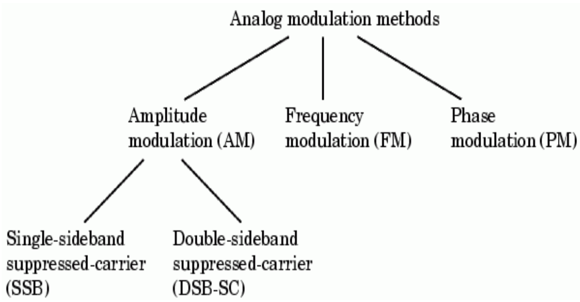

Figure 1: Analog Modulation Techniques

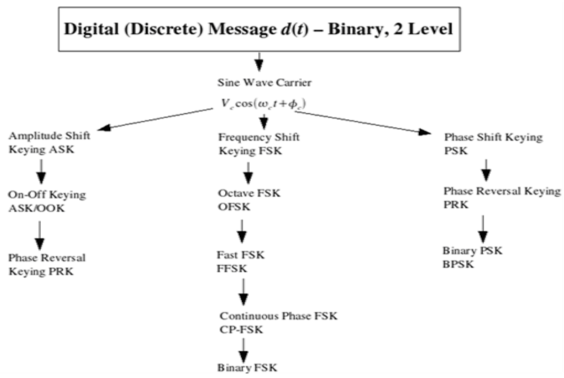

Figure 2: Digital Modulation Techniques

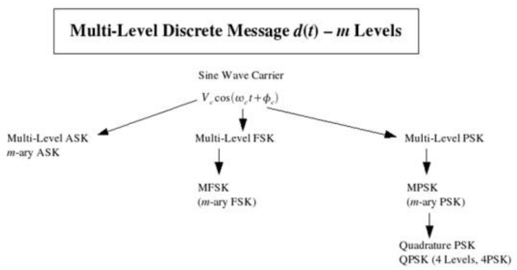

Figure 3: Multi Level Digital Modulation Techniques

DOI 10.17148/IJARCCE.2016.5822

IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319 5940
International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 8, August 2016

B. ENCODING TECHNIQUES

The internal organization of different operations performed between the sending end i.e data link layer and physical layer are as shown in Fig.4. Depending upon the requirement of operation the information in the form of frames of fixed block length is sent from data link layer. These frames are encoded using required encoding technique and the encoded bits are scrambled and sent as a continuous stream of data to the physical layer. Attached sync marker is used to detect the start or end of each data frame.

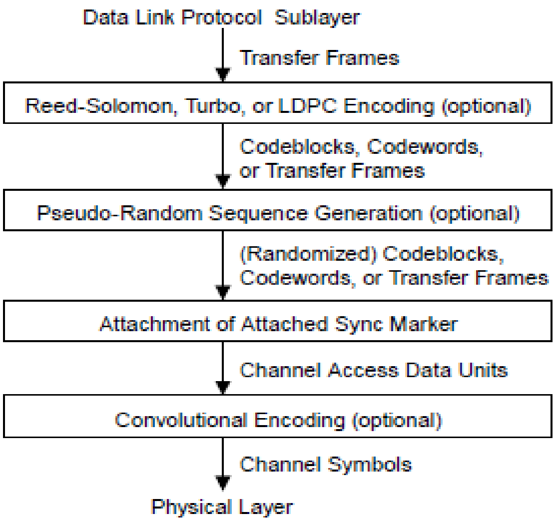

Figure 4: Sub layer organization at Transmitter end

The different types of error controlling coding techniques are

- Convolutional coding
- Turbo coding
- Reed-Solomon coding
- Low density parity check coding

II.QPSK MODULATION SCHEME

The Block Diagram of the QPSK Digital Modulation Scheme is as shown below.

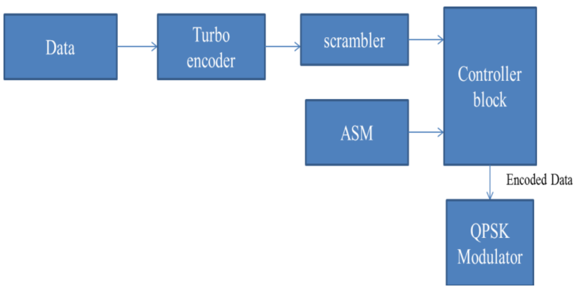

Figure 5: Block Diagram of the QPSK Digital Modulation scheme

At the transmission end, the input data is transmitted in the form of frames each of length 1784 bits. Each bit of the frame is sent serially to the turbo encoder. The turbo encoder encodes each input bit into two bits. The encoded bits are randomized using a scrambler. The controller block controls the working of internal modules. The Attached sync marker of length 64 bits is attached at the starting of each frame to detect the start of each frame of data. The randomized encoded bits are modulated using a Binary Phase Shift Keying modulator.

A.TURBOENCODER

The turbo encoder is the combination of convolution encoders which are connected in parallel. Each encoder consists of four shift registers and gives three outputs based on the generator polynomial connectivity of Ex-or gates.

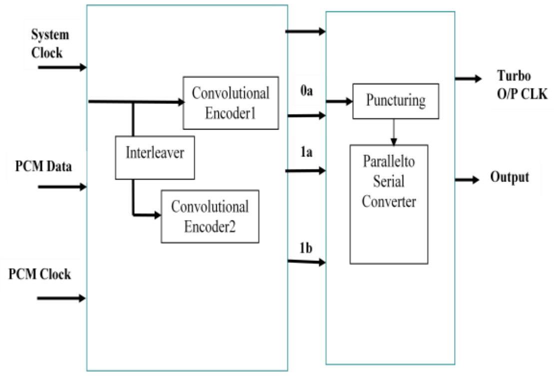

Figure6: Turbo Encoder Block Diagram

Puncturing is done on the encoder outputs in order to obtain required bit rate of 1/2. The punctured code words are arranged in a sequence as shown in Fig.6. The output sequence of the turbo encoder after puncturing is 0a, 1a, 0a, 1b which is represented in the Fig.7.

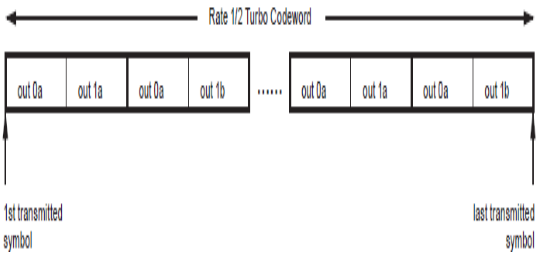

Figure 7: Punctured Code Word for ½ Code Rate

B.INFORMATION BLOCK

Information block represents the data frame of 1784 bits. The signal is used to indicate the end of 1784 bits . The code rates for different information block lengths are listed in the Table.1.

TABLE I. CODE RATES FOR DIFFERENT INFORMATION BLOCK LENGTHS

Information block length k	Codeword length n			
	rate 1/2	rate 1/3	rate 1/4	rate 1/6
1784	3576	5364	7152	10728
3568	7144	10716	14288	21432
7136	14280	21420	28560	42840
8920	17848	26772	35696	53544

IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319 5940
International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 8, August 2016

C. INTERLEAVER

The turbo interleaver modifies the position of each bit of the data frame into another location as shown in Fig.8. In other words, the bit positions are shifted from one location to another location systematically using the below mentioned procedure. It is diagrammatically shown in the Fig.9

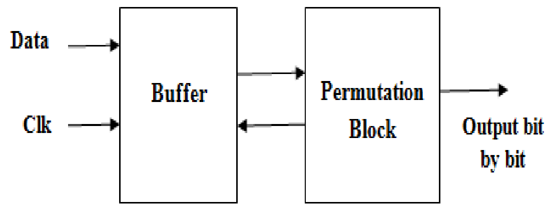

Figure 8: Interleaver Block

D.SCRAMBLER

The polynomial mentioned below is used to generate the pseudo random bits.

$$h(x)=x^8+x^7+x^5+x^3+1$$

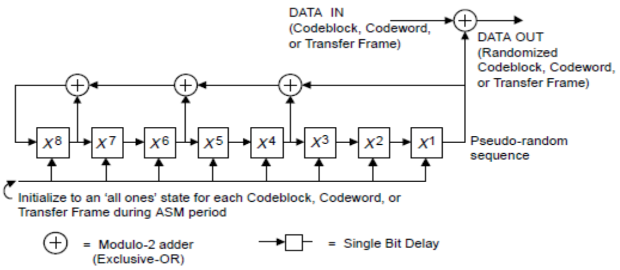

Figure 9: Logic diagram of scrambler

The Fig.9 represents the logic of pseudo randomizer. The scrambler performs the exclusive or operation between nth bit of the encoder output and nth bit of scrambler output to randomize the encoded data.

E.ATTACHED SYNC MARKER(ASM)

Attached Sync Marker(ASM) is attached at the starting of each information block in order to detect the starting position of data frame. Turbo Encoder uses a 64-bit value represented in hex as

034776C7272895B0.

The ASM bits are attached to the scrambled output before modulation process.

F.QPSK MODULATOR

The binary data '00' represents sine wave of phase 225 degrees and the binary data '01' represents sine wave of phase 135 degrees and similarly binary data '10' represents sine wave of 315 degrees and binary data '11'represents sine wave of 45 degrees.

The block diagram of QPSK modulator is shown in the Fig.10. Based on the input bit, the multiplexer modulates the signal as sine 45 or sine 135 or sine 225 or sine 315.

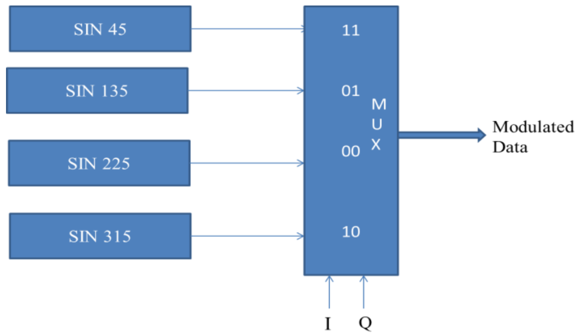

Figure 10: QPSK Modulator

III. SOFTWARE IMPEMENTATION TEST RESULTS

The new simple VHDL Quadrature Phase shift Keying (QPSK) modulator Using Turbo Codes has been synthesized for many Air Borne System Applications.

It is programmed with the Hardware Description Language (VHDL) code to generate the behavioural QPSK digital signal.

The behavioural simulation (RTL view) for QPSK modulator and the Turbo Encoder is shown in the following Figure's.

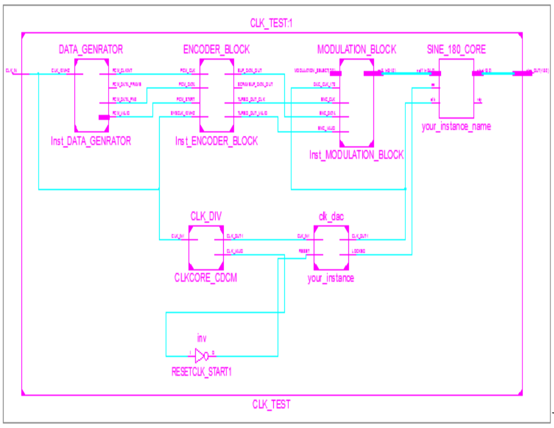

Figure 11: RTL Schematic of QPSK Modulation scheme Top Module

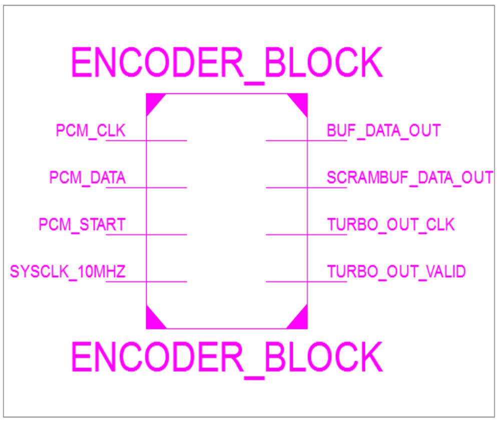

Figure 12: RTL Schematic of Turbo Encoder Block Top Module

IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319 5940
International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 8, August 2016

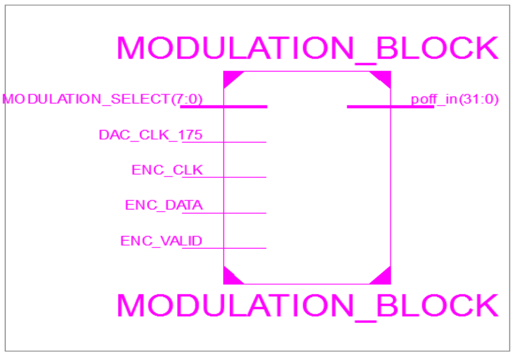

Figure 13 : RTL Schematic of Modulation Block

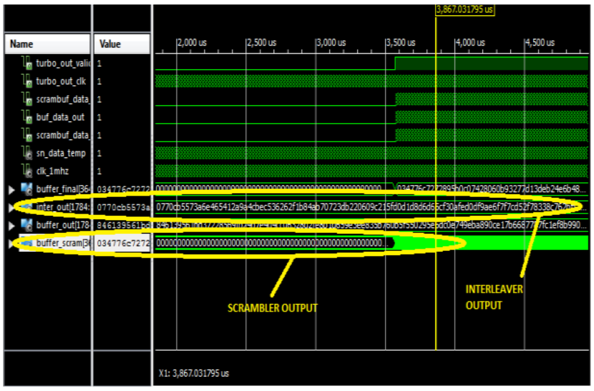

Figure 14: Simulation Result of Turbo Encoder and Scrambler Block

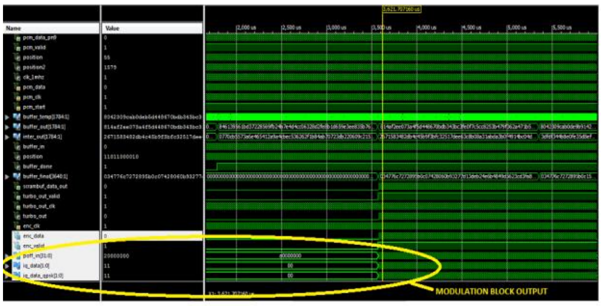

Figure 15: Simulation Result of Modulation Block

IV.HARDWARE IMPLEMENTATION RESULTS

When implemented on the FPGA QPSK modulator circuit whose one output end is given to the Oscilloscope ,we can observe the hardware implementation result as follows

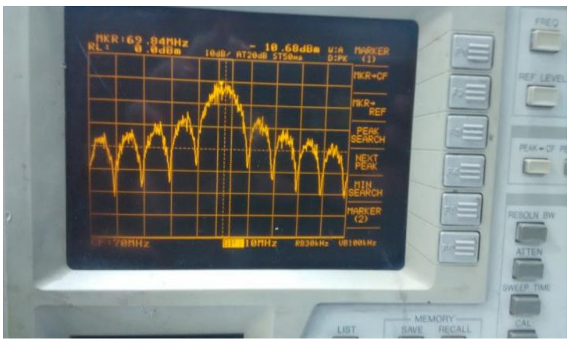

Figure 16: QPSK modulator circuit output in Oscilloscope

V. CONCLUSION

Different techniques are followed by different applications for transmission and reception of data between the physical layer and data link layer. In this study, as per the specifications, for wireless communication with bit rate of 1/2 and frame length of 1784 bits Turbo encoder and QPSK modulator are designed at the transmitting end. These Turbo Encoding and QPSK Modulation techniques are developed as per CCSDS standards and can be applied to long distance communication like space to space or ground to space applications.

ACKNOWLEDGMENTS

An endeavor of a long period can be successful only with The advice of many well-wishers. Authors take this as the Opportunity to express deep gratitude and appreciation to The Head of Department, Department of Electronics and Communication Engineering, G.Pullaiah College of Engineering and Technology, Kurnool, for providing all facilities and all those who encouraged for successful completion of my project work .

REFERENCES

[1] CCSDS ,Recommendation for Space Data System Standards, Blue book, Aug 2011.
[2] CCSDS ,Recommendation for Space Data System Standards, Green book, Nov 2012.
[3] RajibDA,"FPGA implementation of digital modulation schemes", IJECT, Jan ,2014.
[4] GihadElamary, Graeme Chester, "A simple digital VHDL QPSK modulator designed using CPLD/FPGA for biomedical applications", proceedings of WCE,July,2009, U.K.
[5] "Proposed deterministic Interleavers for CCSDS Turbo code standard", journal of theoretical and applied information technology, 2010.
[6] Hina Malik, D.R.Rotake, MamtaMahajan , "Design and Implementation of BPSK Modulator and Demodulator Using VHDL" IOSR Journal of Electronics and Communication Engineering , 2014

BIOGRAPHIES

D. Sai Brunda completed her B.Tech in Electronics & Communication Engineering (ECE) at G. Pullaiah College of Engineering &Technology, Kurnool, India. She is pursuing her M.Tech Degree with specialization in Digital Electronics and Communication Systems (DECS) at G. Pullaiah College of Engineering and Technology, Kurnool, INDIA.

B. Geetha Rani is currently working as an Assistant Professor in G. Pullaiah College of Engineering & Technology, Kurnool, India. She has pursued her M.Tech in Digital Electronics and Communication Systems (DECS) specialization from G. Pullaiah College of Engineering &Technology, Kurnool, India and B.Tech in Electronics & Communication Engineering (ECE) from Sri Kottam Tulasi Reddy College of Engineering &Technology, Kondair, and Mahaboob Nagar, INDIA.